CLAIMS

What is claimed is:

1. ~~A sublamination~~ material, comprising:
a single layer reference ~~plane~~ having a top surface and a bottom surface;
a first signal layer coupled to the top surface ~~with~~ a core material;
a second signal layer coupled to the bottom surface with a ~~bond-ply~~ material; and
at least one of a blind via or a micro via.

2. The sublamination material of claim 1, wherein the reference plane comprises a conductive material.

3. The sublamination material of claim 2, wherein the conductive material is copper.

4. The sublamination material of claim 1, wherein the first signal layer comprises the same material as the second signal layer.

5. The sublamination material of claim 1, wherein the first signal layer is copper.

6. The sublamination material of claim 1, wherein the bond-ply material comprises the same material as the core material.

7. The sublamination material of claim 1, wherein the core material is a dielectric material.

8. The sublamination material of claim 7, wherein the dielectric material is FR4.

9. The sublamination material of claim 1, wherein the second signal layer comprises copper.

10. The sublamination material of claim 1, wherein the bond-ply material is a dielectric material.

11. The sublamination material of claim 10, wherein the dielectric material is BT.

12. The sublamination material of claim 1, wherein the blind via is formed by using a laser or a conventional drill.

13. A method of producing a sublamination material, comprising:
providing a core material, wherein the core material is sandwiched on both sides by a layer of conductive material;
applying a photoresist to the layers of conductive material;

imaging one layer of the conductive material to produce an imaged layer of conductive material;

developing and etching the imaged layer of the conductive material to produce an etched layer of conductive material;

stripping the photoresist from both layers of conductive material;

applying a bonding material to the etched layer of conductive material;

coupling a second metal layer to the bonding material to form a layered stack;

curing the layered stack; and

drilling at least one blind via or micro via into the sublamination material.

14. The method of claim 13, wherein the layer of conductive material is copper.

15. The method of claim 13, wherein the bonding material is FR4.

16. A method for producing an electronic component, comprising:

providing a substrate;

coupling at least one sublamination material to the substrate; and

coupling at least one additional layer to the sublamination material.

17. The method of claim 16, wherein the substrate is a silicon wafer.

18. The method of claim 16, wherein the sublamination material is the sublamination material of claim 1.

19. The method of claim 16, wherein the additional layer is a laminate.

20. The method of claim 16, wherein the electronic component comprises a printed circuit board.